EN-QDD800-DR8

The 800G QSFP-DD800 DR8 Transceiver is designed to transmit and receive serial optical data links up to 106.25 Gbps data rate (per channel) by PAM4 modulation format over single-mode fiber. It is a small-form-factor hot pluggable transceiver module integrated with high performance EML laser. It is compliant with 800G Ethernet specs and QSFP-DD MSA.

Features

- Up to 106.25Gbps data rate per channel by PAM4 modulation
- 8 duplex channels transmitters and receivers
- 8×100G PAM4 EML lasers
- Dual MPO-12 connector receptacle optical interface compliant
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP-DD800 form factor
- Maximum link length of 500m on SMF fiber
- Power consumption: <14W
- International class 1 laser safety certified
- Operating temperature range: 0℃ ~ +70℃
- Compliant with RoHS10

Applications

- 800GBASE-DR8 Ethernet
- Switch & Router Connections
- Data Centers
- Other 800G Interconnect Requirements

Standards

- IEEE Std 802.3cu™-2021
- IEEE Std 802.3ck™-2022
- IEEE Std 802.3df™-2024
- QSFP-DD MSA 6.3
- CMIS Rev 5.1 or later version

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Notes
Transmit characteristics					
Signaling rate	53.125 -50ppm	53.125	53.125 +50ppm	GBd	
Modulation format	PAM4				
Wavelength	1304.5		1317.5	nm	
Side-mode suppression ratio(SMSR)	30			dB	
Average launch power, each lane	-2.9		4	dBm	a,b
Outer Optical Modulation Amplitude (OMAouter), each lane for TDECQ < 1.4 dB	-0.8		4.2	dBm	
for 1.4 dB < TDECQ < 3.4 dB	–2.2 +TDECQ		4.2	dBm	
Transmitter and dispersion eye closure for PAM4(TDECQ)			3.4	dB	
Transmitter eye closure for PAM4 (TECQ)			3.4	dB	
| TDECQ – TECQ |			2.5	dB	
Transmitter overshoot and undershoot			22	%	
Transmitter power excursion			5	dBm	
Extinction ratio	3.5			dB	
Transmitter transition time			17	ps	
Average launch power of OFF transmitter			-15	dBm	
$RIN_{21.4}OMA$			-136	dB/Hz	
Optical return loss tolerance			21.4	dB	
Transmitter reflectance			-26	dB	c
Receive characteristics					
Signaling rate	53.125 -50ppm	53.125	53.125 +50ppm	GBd	
Modulation format	PAM4				
Wavelength	1304.5		1317.5	nm	
Damage threshold	5			dBm	d
Average receive power	-5.9		4	dBm	e
Receive power (OMA_{outer})			4.2	dBm	

Receiver reflectance			-26	dB	

Receiver sensitivity (OMA_{outer}) for TECQ < 1.4 dB			-3.9	dBm	
for 1.4 dB ≤ TECQ ≤ 3.4 dB			TECQ-5.3	dBm	
Stressed receiver sensitivity (OMA_{outer})			-1.9	dBm	f
Conditions of stressed receiver sensitivity test:					g
Stressed eye closure for PAM4 (SECQ), lane under test	3.4			dB	
OMA_{outer} of each aggressor lane	4.2			dBm	

Note a. Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note b. Average launch power of -2.9 dBm corresponds to an OMA of -0.8 dBm with an extinction ratio of approximately 10 dB or an OMA of -0.1 dBm with an extinction ratio of approximately 16 dB.

Note c. Transmitter reflectance is defined looking into the transmitter.

Note d. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.

Note e. Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note f. Measured with conformance test signal at TP3 (see IEEE Std 802.3df™-2024 124.8.10) for the BER specified in IEEE Std 802.3df™-2024 124.1.1.

Note g. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Ordering Information

Part No.	Specifications									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Others	
EN-QDD800-DR8	QSFP-DD 800	800G	EML	-2.9~4dBm	PD	< -3.9dBm @2E-4	0~70 ºC	500m	RoHS	Ethernet

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature	Ts	ºC	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	Vcc	V	-0.3	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature	Tc	ºC	0		70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465
Power Consumption	Pc	W			14

Optical Interface

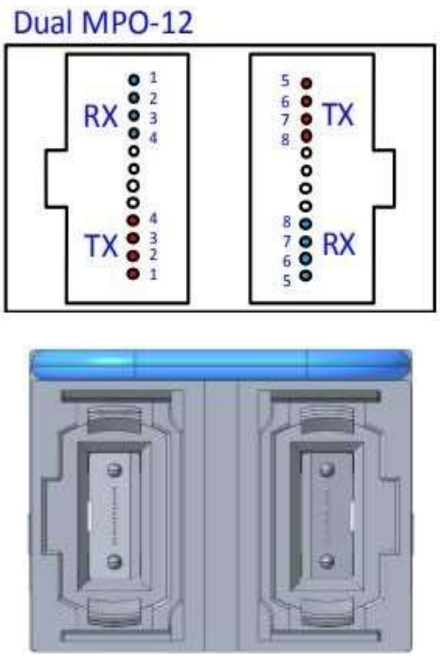

Figure 1 Optical Lane Sequence

Note：Optical interface is 8° APC Dual MPO-12. Lane sequence is shown in Figure 1.

Principle diagram

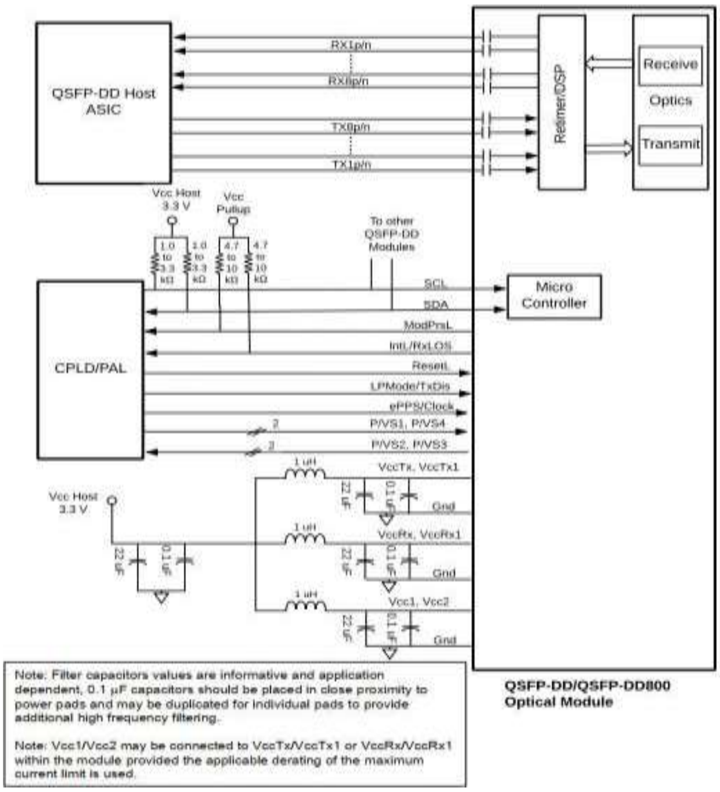

Figure 2 Module Principle Diagram

Electric Ports Definition

Parameter	Min	Typ	Max	Unit	Notes
Supply voltage	3.135		3.465	V	
Signaling rate, each lane	53.125 -100ppm	53.125	53.125 +100ppm	GBd	
Module input characteristics					
Differential peak-to-peak input voltage tolerance	750			mV	TP1a
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCM_{LF}	32			mV	TP1a
Full-band, VCM_{FB}	80			mV	
Differential-mode to common-mode return loss, RLcd	See IEEE Std 802.3ck™-2022 Equation(120G-2)			dB	TP1

Effective return loss, ERL	8.5			dB	TP1

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Parameter	Min	Typ	Max	Unit	Notes
Differential termination mismatch			10	%	TP1
Module stressed input tolerance	See IEEE Std 802.3ck™-2022 120G.3.4.3				TP1a
Single-ended voltage tolerance	-0.4		3.3	V	TP1a
DC common-mode voltage tolerance	-0.35		2.85	V	TP1
Module output characteristics					
Peak-to-peak AC common-mode voltage Low-frequency, VCM_{LF}			32	mV	TP4
Full-band, VCM_{FB}			80	mV	
Differential peak-to-peak output voltage Short mode			600	mV	TP4
Long mode			845	mV	
Eye height	15			mV	TP4
Vertical eye closure, VEC			12	dB	TP4
Common-mode to differential-mode return loss, RLdc	See IEEE Std 802.3ck™-2022 Equation(120G-1)			dB	TP4
Effective return loss, ERL	8.5			dB	TP4
Differential termination mismatch			10	%	TP4
Transition time	8.5			ps	TP4
DC common-mode voltage tolerance	-0.35		2.85	V	TP4
IIC communication					
IIC Clock frequency	100		1000	kHz	
Clock stretching			500	µs	
Data In Hold Time	0			µs	
Data In Setup Time	0.1			µs	

Pin Description

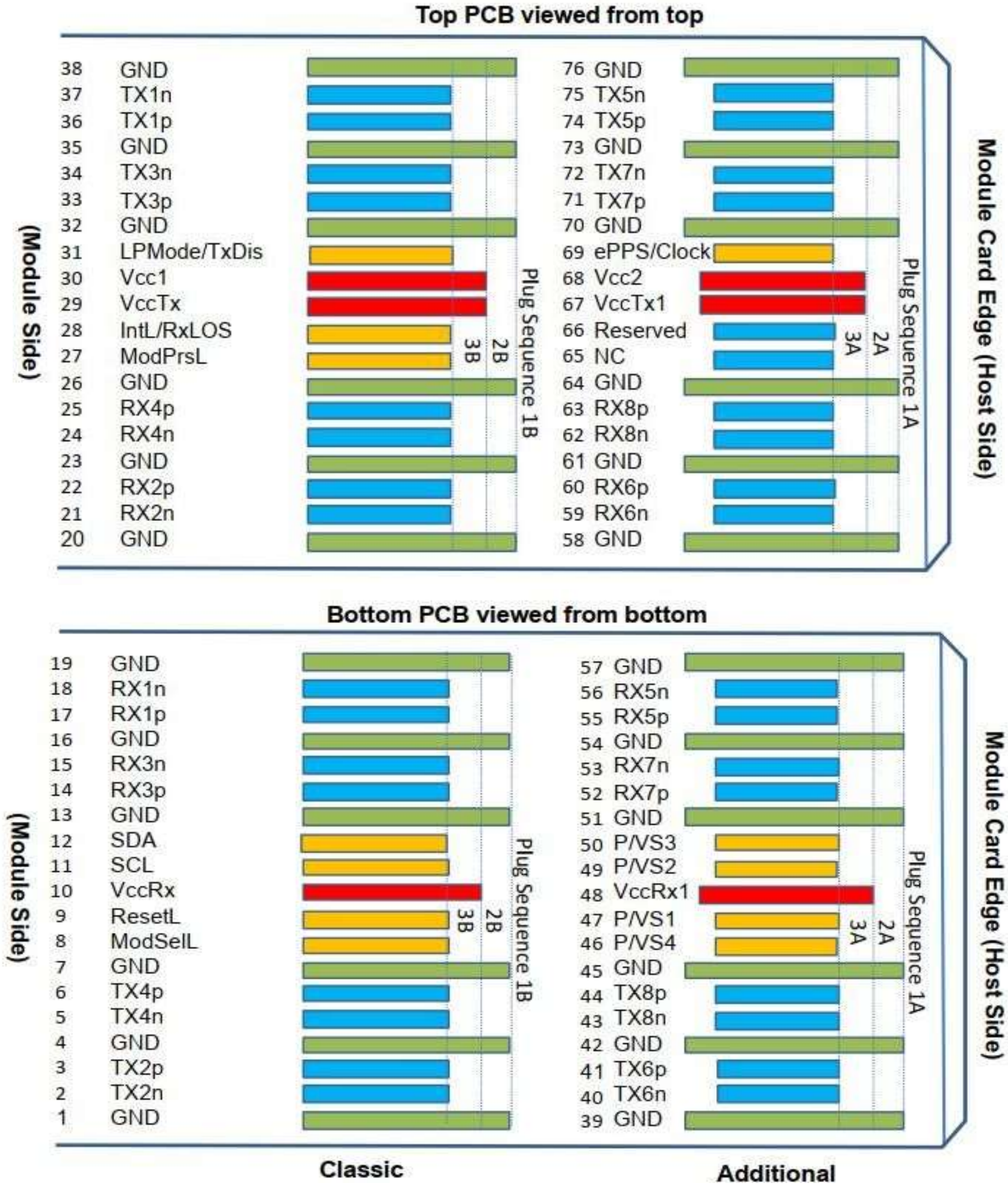

Figure 3 Module pad assignment and layout

Pad	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Intput	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	TWI serial interface clock	
12	LVCOMS-I/O	SDA	TWI serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	

Pad	Logic	Symbol	Description	Notes
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	5
48		VccRx1	+3.3V Power Supply	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	5
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	

Pad	Logic	Symbol	Description	Notes
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		VccTx1	+3.3 V Power Supply	2
68		Vcc2	+3.3 V Power Supply	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	6
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in QSFP-DD MSA Specification Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500mA.

Note 3: Reserved pad recommended to be terminated with 10kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10kΩ to ground on the host.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10kΩ.

Note 6: For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module see QSFP-DD MSA Specification clause 4.2.6.

Module Memory Map

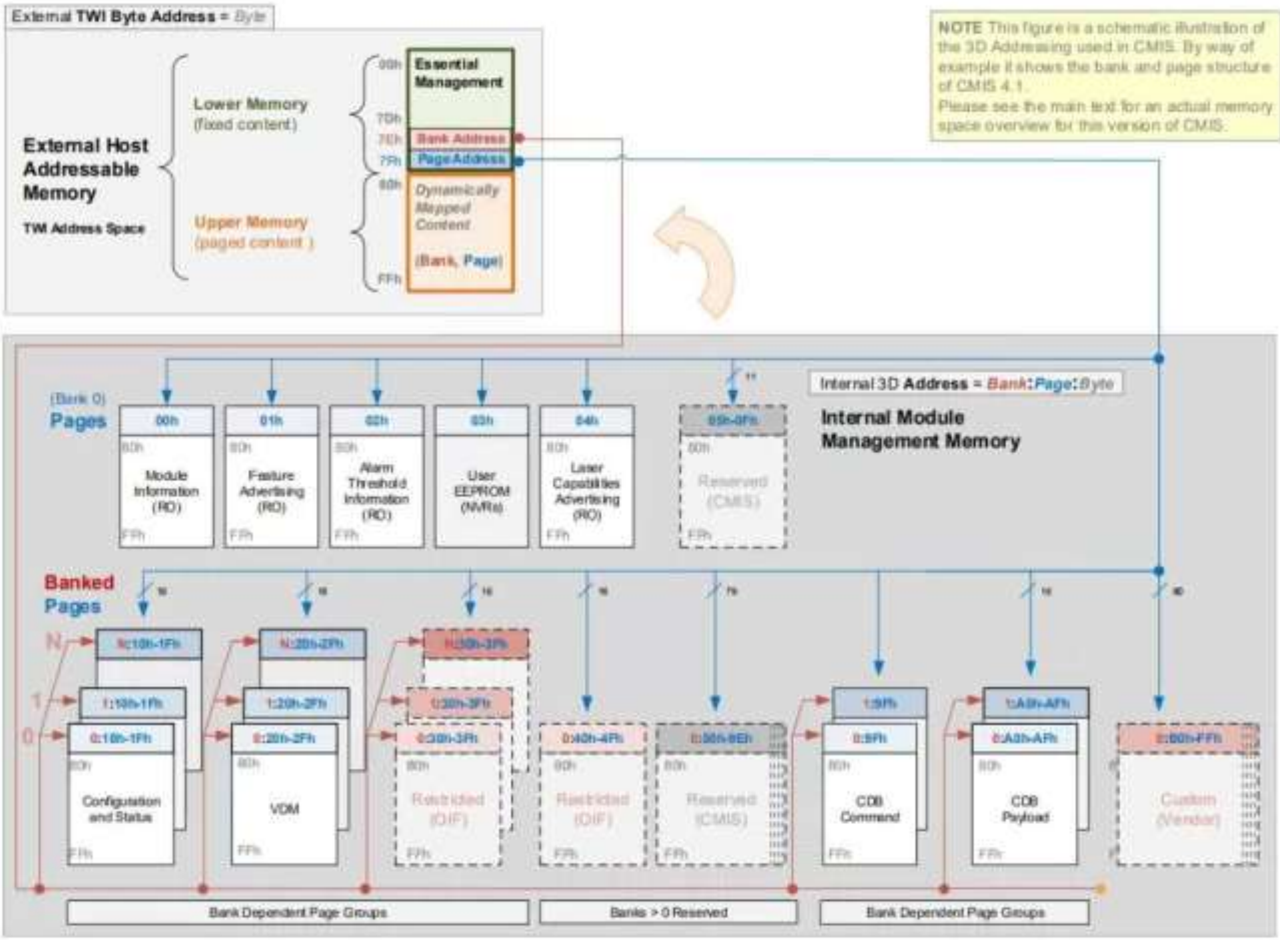

Figure 4 Digital Diagnostic Memory Map

Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. System designers should choose components with appropriate DCR and ESR, to minimize the voltage drop and the amount of noise coupled to the module. Hosts supporting higher power classes modules may require additional design considerations, in order to minimize the voltage drop and the amount of noise coupled to the module.

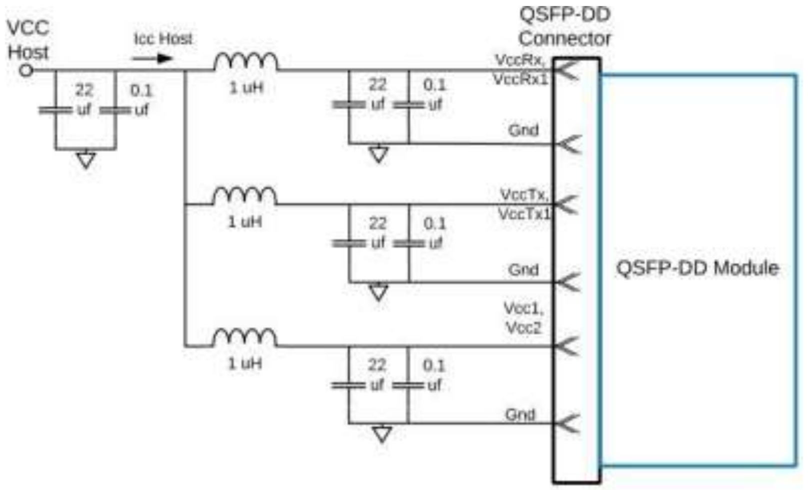

Figure 5 Reference Power Supply Filter for Module Testing

Package Outline

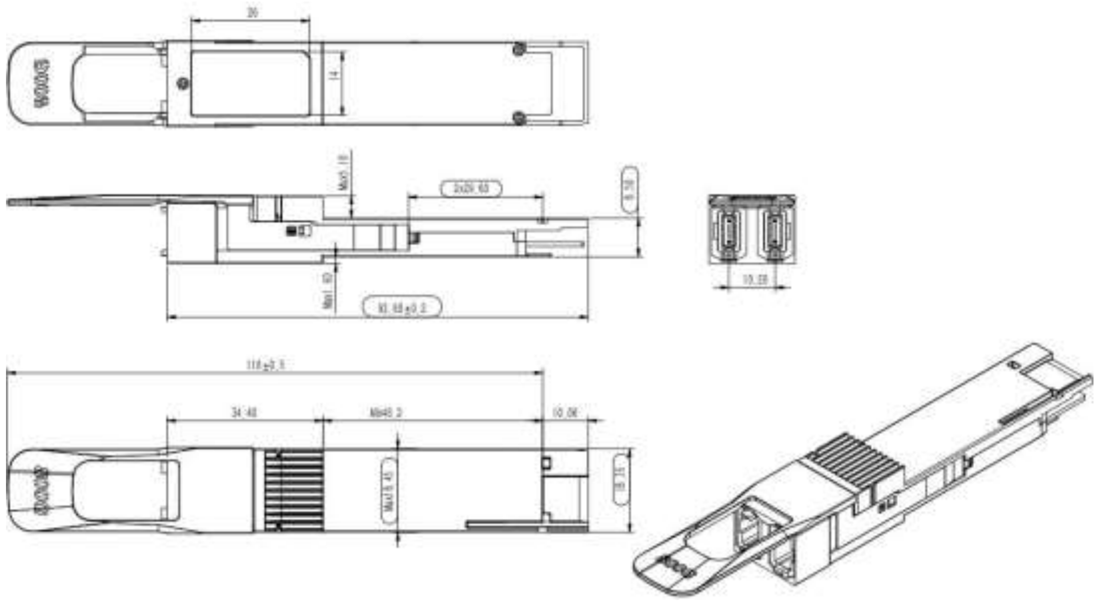

Figure 6 Package Outline