EN-QDD800-2LR4-2CS

800G QSFP-DD 2xLR4 Transceiver 10KM 0-70℃

Features

- Up to 10Km transmission distance
- Signaling rate per lane, 53.125GBd
- EML with TEC and PIN receiver
- Modulation format, PAM4
- 400GAUI-4 electrical interface
- 2-wire interface for integrated Digital Diagnostic monitoring
- QSFP-DD MSA package with dual CS connectors
- Hot pluggable
- Very low EMI and excellent ESD protection
- +3.3V power supply
- Power consumption less than 16W
- Operating case temperature: 0~70℃

Applications

- 2x400GBASE-LR4

Compliance

- Compliant with IEEE802.3 cu-2021
- Compliant with QSFP-DD-Hardware-rev6.3
- Compliant with QSFP-DD-CMIS-rev5.2
- Compliant with RoHS-6

Description

The E.C.I. NETWORKS EN-QDD800-2LR4-2CS is a high-performance, cost-effective module for optical data communication applications to 800G and transmission distance up to 10km on SM fiber. The transceiver consists of two sections: The transmitter section incorporates two quad channel EML Laser, two quad channel driver and a DSP. The receiver section consists of two quad channels PIN photodiode integrated with two quad channel transimpedance preamplifier (TIA) and sharing DSP with transmitter. The module is hot pluggable with a 76-pin connector. The high-speed electrical interface is based on low voltage logic, with nominal 100 Ohms differential impedance and AC coupled in the module.

The EN-QDD800-2LR4-2CS converts 8-channel 106.25Gb/s(PAM4) electrical data to 8-channel 106.25Gb/s optical signals and multiplex them into two single mode fibers for 450Gb/s optical transmission with CS connector. Similarly, it optically de-multiplexes two 450Gb/s input into 8-channel signals, and converts them 8-channel output electrical data on the receiver side. The module offers very high functionality and feature integration, accessible via a two-wire serial interface. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Absolute Maximum Ratings

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	℃
Supply Voltage （no damaged）	V_{CC}	-0.5	3.6	V
Relative Humidity(non-condensing)	RH	5	85	%
Damage threshold	P	6.1		dBm

Recommended Operating Conditions

Table2-Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	0		70	℃
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V
	I_{CC}			5104	mA
Maximum sustained peak Current(<500ms)				5281	mA
Maximum Instantaneous peak current(<50us)				6400	mA
Electro-Static discharge	ESD	1000	-	-	V
Power Dissipation	P_D			16	W
Signaling rate, each lane			106.25		Gbps
Transmission Distance				10	Km

Optical｜Electrical Characteristic

EN-QDD800-2LR4-2CS (CWDM EML and PIN, 10Km)

Tested under recommended operating conditions, unless otherwise noted

Table3-Transmitter Operating Characteristic-Optical，Electrical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Optical Interface Parameters						
Centre Wavelength	λ_C	1264.5	1271	1277.5	nm	
		1284.5	1291	1297.5	nm	
		1304.5	1311	1317.5	nm	
		1324.5	1331	1337.5	nm	
Modulation format		PAM4				
Signaling rate, each lane			53.125		GBd	
Side Mode Suppression Ratio	SMSR	30			dB	
Total average launch power(max)	P_{tot}			11.1	dBm	

Average Optical Power each lane	P_{avg}	-2.7		5.1	dBm	
Optical Modulation Amplitude each lane	P_{OMA}	0.3		4.4	dBm	Note1
		-1.1+TDECQ		4.4	dBm	Note2
Extinction Ratio	ER	3.5			dB	
Difference in launch power between any two lanes(Average and OMA)				4	dB	
Transmitter and Dispersion eye closure for PAM4(TDECQ) each lane	TDECQ			3.4	dB	
Relative Intensity Noise	$RIN_{15.6}OMA$			-136	dB/Hz	
Average launch power of OFF transmitter, each lane (max)	P_{off}			-30	dB	
Optical Return Loss Tolerance		-		15.6	dB	
Transmitter reflectance (max)				-26	dB	
Electrical Interface Parameters						
Differential peak-to-peak output voltage Transmitter disabled Transmitter enabled				35 750	mV	
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB				32 80	mV	
Eye height		10			mV	
Vertical eye closure, VEC				12	dB	
Transition time Host is requesting short mode Host is requesting long mode		10 15			ps	

Notes:

[1] For TDECQ＜1.4dB.

[2] For 1.4≤TDECQ≤3.4dB.

Table4-Receiver Operating Characteristic-Optical , Electrical

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Optical Interface Parameters						
Center Wavelength	λr	1264.5	1271	1277.5	nm	
		1284.5	1291	1297.5	nm	
		1304.5	1311	1317.5	nm	
		1324.5	1331	1337.5	nm	

Modulation format		PAM4				
Signaling rate, each lane			53.125		GBd	
Average receive power, each lane(EOL)		-9		5.1	dBm	
Receive power (OMA outer), each lane (max)				4.4	dBm	
Difference in receive power between any two lanes (OMA) (max)				4.3	dB	
Receiver sensitivity OMA outer each lane				max(-6.8 ,SECQ-8. 2)	dBm	Note 1
Receiver Overload (Average power), each lane(min)		5.1			dBm	
Stress Sensitivity OMA outer (each Lane)				-4.8	dBm	
LOS Assert	LosA	-20			dBm	
LOS Dessert	LosD			-10.8	dBm	
Receiver Reflectance				-26	dB	

Notes:

[1] Measured with conformance test signal at TP3 for the BER specified in 124.1.1 802.3-2018.

Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

Table5- Digital Diagnostic Functions

Parameter	Symbol	Min.	Max.	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3	3	℃	Over operating temp
Laser power monitor absolute error	DMI_TX	-3	3	dB	
RX power monitor absolute error	DMI_RX	-3	3	dB	
Supply voltage monitor absolute error	DMI_VCC	-3	3	%	
Bias current monitor absolute error	DMI_Ibias	-10	10	%	
No-power monitor RX		-40		dBm	
Tx_disable power monitor		-40		dBm	

Table6-Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit	Note
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Note1
ResetL Assert Time	t_reset_init	10		us	Note2
IntL Assert Time	ton_IntL		200	ms	Note3
IntL Deassert Time	toff_IntL		500	us	Note4

Tx Fault Assert Time	ton_Txfault		200	ms	Note5
Flag Assert Time	ton_flag		200	ms	Note6
Software Tx Disable Assert Time	ton_TxDisf		100	ms	Note7
Software Tx Disable Deassert Time	toff_TxDisf		400	ms	Note8
Rx Squelch Assert Time	ton_rxsq		15	ms	
Rx Squelch Deassert Time	toff_rxsq		5	s	
Rx Squelch Assert Time	ton_rxsq		15	ms	
Rx Squelch Deassert Time	toff_rxsq		5	s	

Notes:

[1] Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.

[2] Minimum pulse time on the ResetL signal to initiate a module reset.

[3] Time from occurrence of condition triggering IntL until Vout:IntL=Vol.

[4] Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.

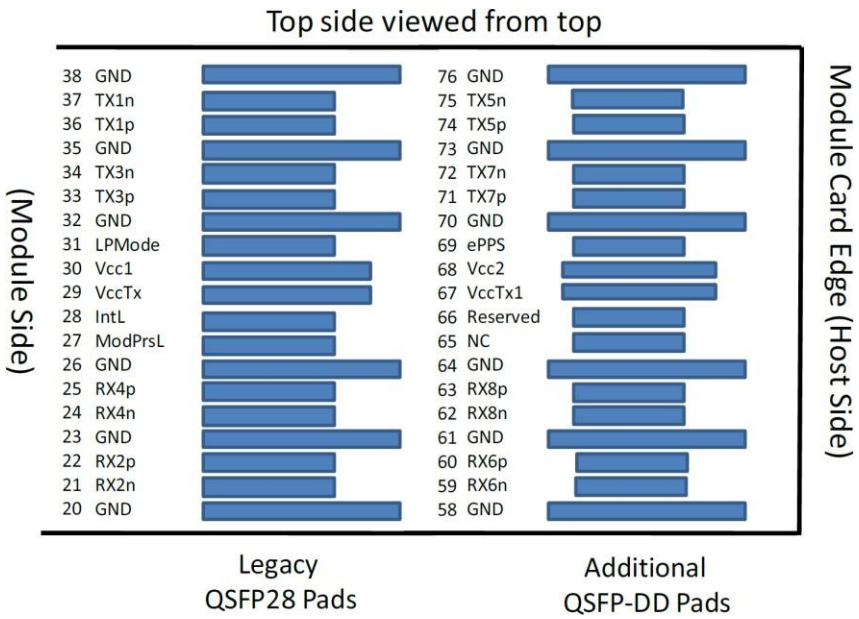
[5] Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.

[6] Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.

[7] Time from Tx Disable bit set (value = 1b) until optical output rises above 90% of nominal.

[8] Time from Tx Disable bit cleared (value = 0b) until optical output rises above 90% of nominal.

Pin-out Definitions



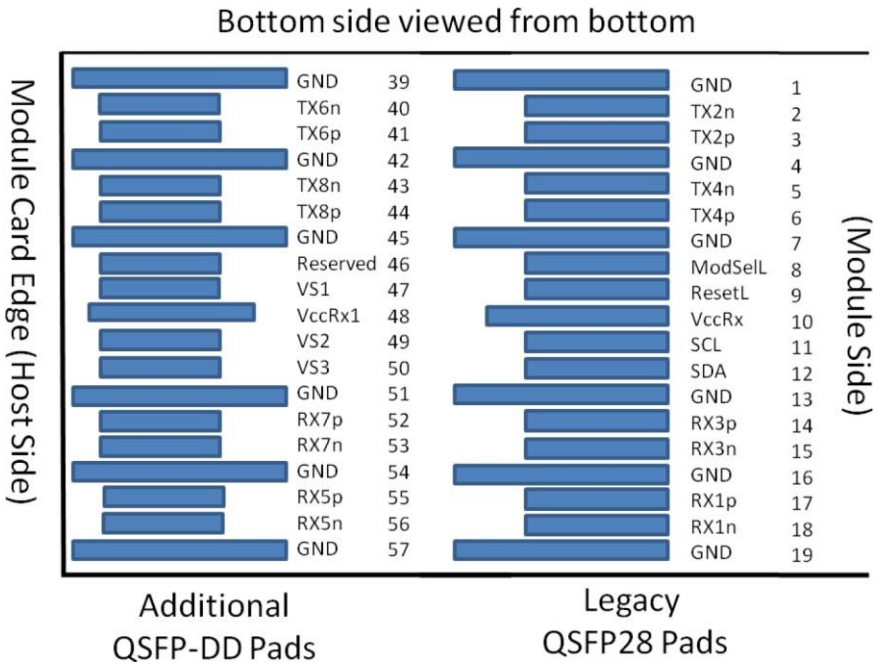


Figure1 MODULE PAD LAYOUT

Table7-Pin Function Definitions

Pin	Logic	Symbol	Name/Description	Plug Sequence[4]	Note
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	

19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	

57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

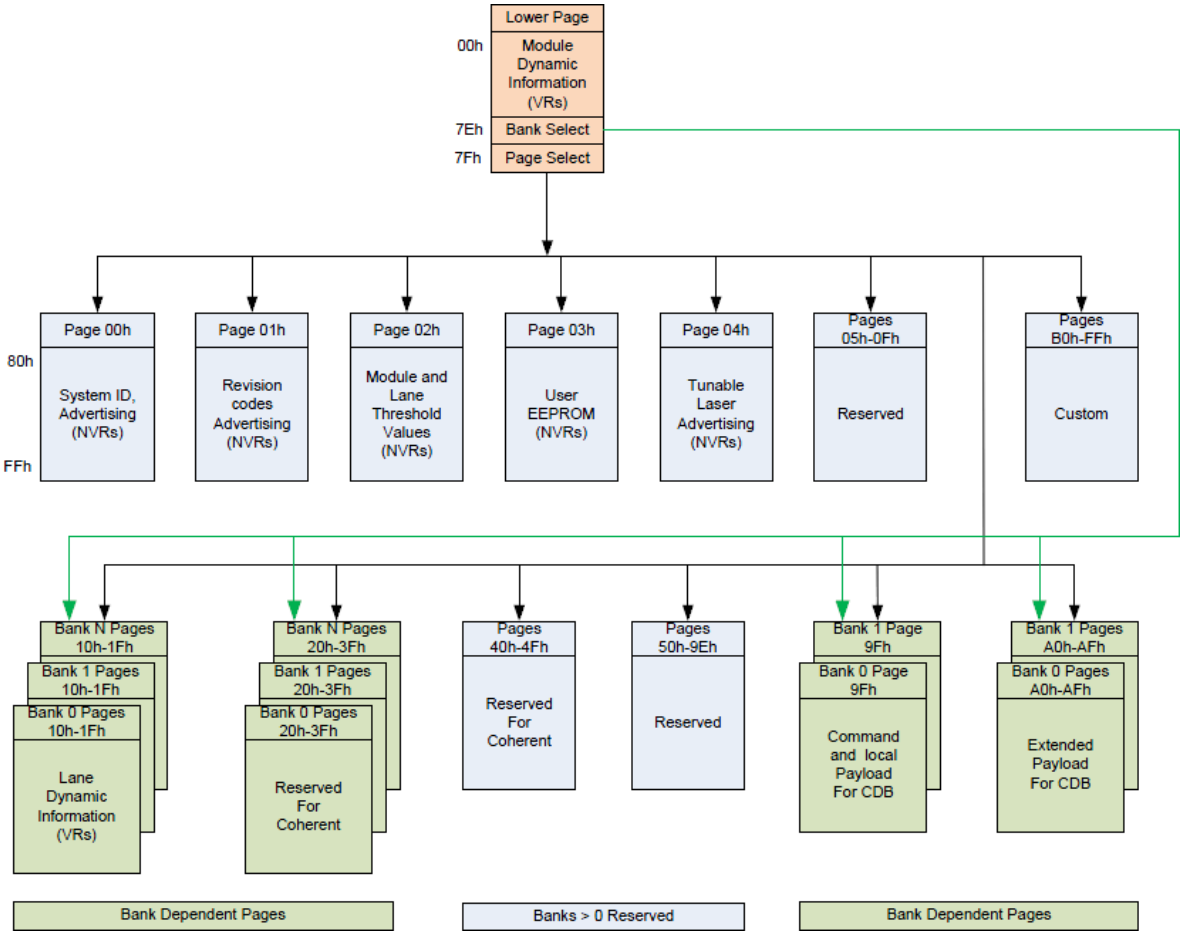
[1] QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

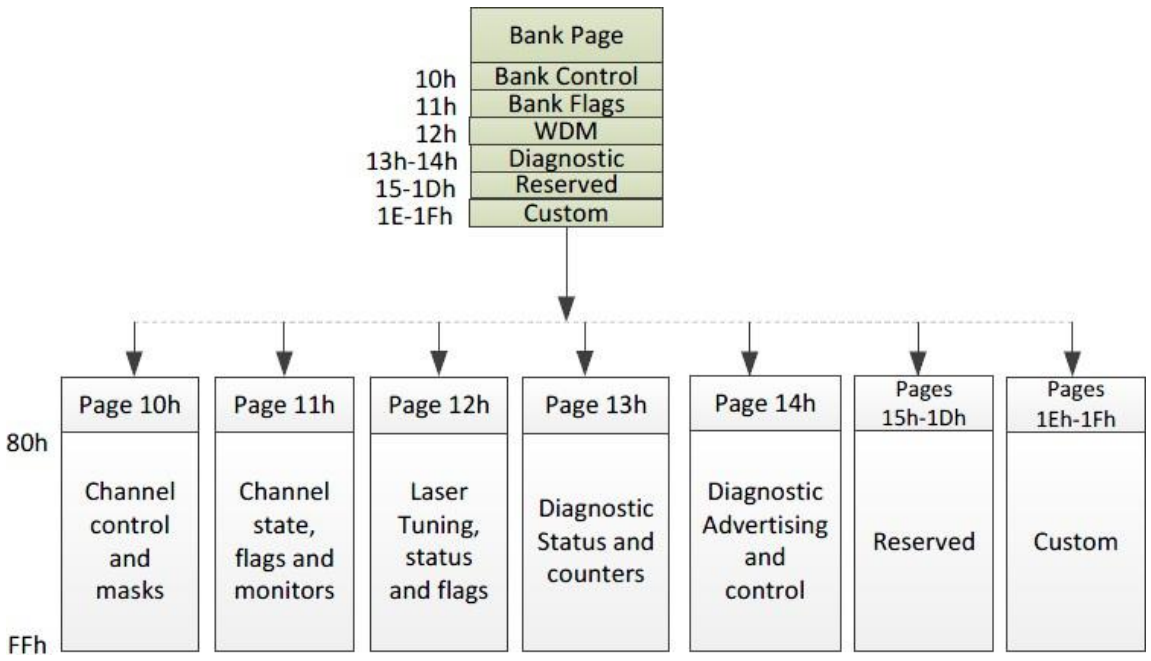
[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

Digital Diagnostic Memory Map





EEPROM Information

The QSFP-DDmgmt defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2-wire serial interface. The memory contents refer to Table 8.

Table8-EEPROM Serial ID Memory Contents (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
0	1	Identifier	18	QSFP-DD
1	1	Revision Compliance	52	CMIS Rev5.2
2	1	Flate_men/CLEI/TWI max speed		
3	1	Module state/interrupt		
4-7	4	Bank lane Flag Summary		
8	1	firmware fault & L-Module state change flag		
9	1	3.3V&temperture low/high alarm/warning flag		
10	1	L-Aux1 &L-Aux2 low/high alarm/warning flag		
11	1	L-Vendor define & L-Aux3 low/high alarm/warning flag		
12	1	Reserved		
13	1	Custom		
14-25	12	Module Monitors		
26	1	LowPwr /Squelch control / ForceLowPwr/soft reset	40	
27-28	2	Reserved	00 00	
29-30	2	Custom	00 00	
31-36	6	Module masks	00 00 00 00 00 00	
37-38	2	CDB Status Area		
39-40	2	Module Firmware Version	01 00	
41-63	27	Reserved	00	
64-84	21	Custom	00	
85	1	MODULE TYPE CODE	02	SMF

86-117	32	module host-media interface	52 43 88 01 50 43 44 11 FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Support 1x800G and 2x400G
118-121	3	password Change Area	00 00 00 00	
122-125	4	Password Area	00 00 00 00	
126	1	Bank Select Byte	00	
127	1	Page Select Byte	00	
128	1	Identifier	18	QSFP-DD
129-144	16	Vendor name	48 47 20 47 45 4E 55 49 4E 45 20 20 20 20 20 20	E.C.I. NETWORKS
145-147	3	Vender OUI	DA 28 EC	
148-163	16	Vender PN	4D 51 44 2D 47 37 46 36 43 20 20 20 20 20 20 20	EN-QDD800-2LR4-2CS
164-165	2	Vender rev	31 300	
166-181	15	Vender SN	Variable	
182-189	8	Data Code	Variable	
190-199	10	CLEI Code	20 20 20 20 20 20 20 20 20 20	
200-201	2	Module power characteristics	E0 40	POWER CLASS 8 (16W) MAXPOWER 16W
202	1	Cable assembly length	00	
203	1	Media Connector Type	25	CS
204-209	6	Copper Cable Attenuation	00 00 00 00 00	
210-211	2	Cable Assembly Lane Information	00 00	
212	1	Media Interface Technology	06	
213-220	8	Reserved	00 00 00 00 00 00 00 00	
221	1	Custom	00	
222	1	Checksum	Variable	
223-255	33	Custom Info NV	00	

Ordering Information

Table9- Ordering Information

Part No.	Specification									Application
	Pack	Rate	Tx	Pout	Rx	Sens_OMA	Top	Reach	Others	
EN-QDD800-2LR4-2CS	QSFP-DD	800G	CWDM EML	-2.7~5.1dBm	PIN	＜-6.8dBm	0～70℃	10km	DDM/RoHS	800G 2xLR4

Notice:

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